Amendments to the Claims:

This listing of the claims will replace all prior versions and listings of the claims in the application:

1. (Previously Presented) A method for testing a semiconductor memory device including nm memory cell arrays for respectively outputting x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1, the method comprising:

extending y-bit data received through y data I/O pads to (nm×x)-bit data to write the x-bit data to each of the nm memory cell arrays in a test data write step; and

comparing the x-bit data output from each of the nm memory cell arrays to generate nm-bit comparison result data, and sequentially outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively, in a test data read step.

2. (Previously Presented) The method of Claim 1, wherein in the test data write step, when the x-bit data is written to the respective nm memory cell arrays, the x-bit data written to the respective nm memory cell arrays are same-bit data.

3. (Previously Presented) The method of Claim 1, wherein the test data read step further comprises:

respectively comparing the x-bit data output from each of the nm memory cell arrays to generate the nm-bit comparison result data in a comparing step; and

outputting the y-bit comparison result data selected by selecting, by y bits, the nm comparison result data in response to the control signal to the y data I/O pads in a selecting step.

4.-9. (Canceled).

10. (Previously Presented) A method for testing a semiconductor memory device including nm memory cell arrays for respectively outputting x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1, the method comprising:

extending y-bit data received through y data I/O pads to (nm×x)-bit data to write the x-bit data to each of the nm memory cell arrays wherein nm is integer times as greater as y in a test data write step; and

comparing the x-bit data output from each of the nm memory cell arrays to generate nm-bit comparison result data, grouping and outputting the nm-bit comparison result data into y groups by bit data generated with respect to corresponding n word lines or with respect to corresponding m column selecting signal lines in response to a control signal, and outputting y-bit comparison result data generated by respectively comparing the y grouped bit data through the y data I/O pads in a test data read step.

11. (Currently Amended) A semiconductor memory device, comprising:

nm memory cell arrays configured to respectively output x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1;

a test data write circuit configured to extend y-bit data received through y data I/O pads to (nm×x)-bit data to write the x-bit data to each of the nm memory cell arrays; and

a test data read circuit configured to compare the x-bit data output from each of the nm memory cell arrays to generate nm-bit comparison result data, and sequentially output y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively.

12. (Previously Presented) The device of Claim 11, wherein in the test data write circuit, when x-bit data is written to the respective nm memory cell arrays, the x-bit data written to the respective nm memory cell arrays are same-bit data.

13. (Previously Presented) The device of Claim 11, wherein the test data read circuit includes:

a comparator configured to respectively compare the x-bit data output from each of the nm memory cell arrays to generate the nm-bit comparison result data; and

a selecting circuit configured to output the y-bit comparison result data selected by selecting, by y bits, the nm comparison result data in response to the control signal to the y data I/O pads.

14.-20. (Canceled).

21. (Previously Presented) A semiconductor memory device, comprising:

nm memory cell arrays configured to respectively output x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1;

a test data write circuit configured to extend y-bit data received through y data I/O pads to (nm×x)-bit data to write the x-bit data to each of the nm memory cell arrays wherein nm is integer times as greater as y; and

a test data read circuit configured to compare the x-bit data output from each of the nm memory cell arrays to generate nm-bit comparison result data, group and output the nm-bit comparison result data into y groups by bit data generated with respect to corresponding n word lines or with respect to corresponding m column selecting signal lines in response to a control signal, and output y-bit comparison result data generated by respectively comparing the y grouped bit data through the y data I/O pads.

22. – 36. (Canceled).

37. (Previously Presented) The device of claim 21, wherein the test data read circuit includes:

a first comparator configured to respectively compare the x-bit data output from each

of the nm memory cell arrays;

a selecting circuit configured to group and output the nm-bit comparison result data into y groups by bit data generated with respect to corresponding n word lines or with respect to corresponding m column selecting signal lines in response to the control signal; and

a second comparator configured to output the y-bit comparison result data generated by respectively comparing the y grouped bit data through the y data I/O pads.

38. (Previously Presented) The device of claim 37, wherein y is set to at least n when n is greater than m and is set to at least m when m is greater than n.

39. (Previously Presented) The method of claim 10, wherein in the test data write step, when x-bit data are written to the respective nm memory cell arrays, the x-bit data written to the nm memory cell arrays are same-bit data.

40. (Previously Presented) The method of claim 39, wherein the test data read step further comprises:

respectively comparing the x-bit data output from each of the nm memory cell arrays in a first comparing step;

grouping and outputting the nm-bit comparison result data into y groups by bit data generated with respect to corresponding n word lines or with respect to corresponding m column selecting signal lines in response to a control signal; and

outputting the y-bit comparison result data generated by respectively comparing the y grouped bit data through the y data I/O pads.

41. (Previously Presented) The method of claim 40, wherein y is set to at least n when n is greater than m and is set to at least m when m is greater than n.